

FORM PT01449  
(REV. 8-83)

U.S. DEPARTMENT OF COMMERCE  
PATENT AND TRADEMARK OFFICE

ATTY. DOCKET NO.

HARI.006USE

SERIAL NO.

08/771,708

INFORMATION DISCLOSURE STATEMENT

(Use several sheets if necessary)

APPLICANT

Eliyahou Harari et al.

FILED

December 20, 1996

GROUP

2785

U. S. PATENT DOCUMENTS

*EXAMINER INITIAL	DOCUMENT NUMBER	DATE	NAME	CLASS	SUB CLASS	FILING DATE
LWH	A29 4 1 8 1 9 8 0	1/1980	McCoy	365	1854	
LWH	A30 4 2 7 2 8 3 0	6/1981	Moench	365	45	
LWH	A31 4 2 8 7 5 7 0	9/1981	Stark	365	104	
LWH	A32 4 5 8 6 1 6 3	4/1986	Koike	365	104	
LWH	A33 4 6 5 3 0 2 3	3/1987	Suzuki et al.	365	104	
LWH	A34 4 8 4 7 8 0 8	7/1989	Kobatake	365	104	

FOREIGN PATENT DOCUMENTS

DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB CLASS	TRANS.? (YES/NO)

OTHER DOCUMENTS (Including Author, Title, Date, Pertinent pages, Etc.)

LWH	C21	Stark, M., "Two Bits Per Cell Rom," IEEE Catalog No. 81-CH1626-1, Library of Congress No. 80-85186, Order No. 341, Spring Comp Con 1981, Feb. 23-26, Twenty-Second Computer Society International Conference, San Francisco, CA
LWH	C22	Furuyama et al., "An Experimental 2-Bit/Cell Storage Dram For Macro Cell Or Memory-On-Logic Application," pp. 4.4.1 - 4.4.4, IEEE, (1988)
LWH	C23	Horiguchi et al., "An Experimental Large-Capacity Semiconductor File Memory Using 16-Level Cell Storage," IEEE Journal Of Solid-State Circuits, Vol. 23, No. 1, February 1988

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*EXAMINER INITIAL	DOCUMENT NUMBER	DATE	NAME	CLASS	SUB CLASS	FILING DATE
LW	A1 4 0 9 0 2 5 8	5/1978	Cricchi	365	184	
LW	A2 4 1 4 9 2 7 0	4/1979	Cricchi et al.	365	222	
LW	A3 4 2 7 9 0 2 4	7/1981	Schrenk	365	185.22	
LW	A4 4 3 5 7 6 8 5	11/1982	Daniele et al.	365	185.22	

**FOREIGN PATENT DOCUMENTS**

DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB CLASS	TRANS.? (YES/NO)
B1 2 0 6 1 6 5 1 B	1981	United Kingdom			
B2 5 9 3 1 1 5 8	1984	Japanese Pat. Publica.			YES

**OTHER DOCUMENTS (Including Author, Title, Date, Pertinent pages, Etc.)**

LW	C1	Torelli et al., "An improved method for programming a word-erasable EEPROM," Alta Frequenza, Vol. LII, No. 6, pp. 487-494, Nov.-Dec. 1983
LW	C2	Torelli et al., "Single Chip, 16-Station TV Digital Tuning System," SGS-ATES Technical Note 170, pp. 1-19 (1984)
LW	C3	Torelli et al., "PLL2K-PLL Frequency Synthesizer For 30 Programs," SGS-ATES Componenti Electronici SpA, Technical Note 152, pp. 1-16 (1982)
LW	C4	Scrocchi et al., "EPM32-Electronic Program Memory System For TV (32 Stations)," SGS-ATES Componenti Electronici SpA, Technical Note 153, pp. 1-19 (1982)
LW	C5	"EPM 16-Electronic Program Memory (16 Stations)," SGS-ATES Componenti Electronici SpA, MOS Integrated Circuits/M193A-M193C-M193D, 15 pps, (November, 1981)
LW	C6	"EPM-32 Electronic Program Memory (32 Stations)," SGS-ATES Componenti Electronici SpA, MOS Integrated Circuits/M293, 16 pps. (October, 1982)
LW	C7	"Single Chip Non-Volatile Station Memory, PCM Remote Control Receiver and Display Driver," SGS-ATES Componenti Electronici SpA, MOS Integrated Circuits/M490-M491, 24 pps. (May, 1983)

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LWH	A5	4 5 9 9 7 0 7	7/1986	Fang	365	185.02	
LWH	A6	4 7 1 8 0 4 1	8/1988	Baglee et al.	365	185.22	
LWH	A7	4 7 6 3 3 0 5	8/1988	Kuo	365	185.22	
LWH	A8	4 8 0 5 1 5 1	2/1989	Terada et al.	371	21.1	
LWH	A9	4 8 1 1 2 9 4	3/1989	Kobayashi et al.	365	185.22	
LWH	A10	5 0 5 3 9 9 0	10/1991	Kreifels et al.	711	103	
	A11	<del>5 0 9 5 3 4 4</del>	<del>1992</del>	<del>Harari</del>			

## FOREIGN PATENT DOCUMENTS

		DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB CLASS	TRANS.? (YES/NO)
LWH	B3	6 2 2 5 7 6 9 9	1987	Japan			Abstr

## OTHER DOCUMENTS (Including Author, Title, Date, Pertinent pages, Etc.)

LWH	C8	"PLL TV Microcomputer Interface," SGS-ATES Componenti Electronici SpA, MOS Integrated Circuits/M290, 15 pps. (June, 1982)					
LWH	C9	Gee et al., "An Enhanced 16K E <sup>2</sup> PROM," <u>IEEE Journal of Solid State Circuits</u> , Vol. SC-17, No. 5 (Oct. 1982)					
LWH	C10	Torelli, "An LSI technology fully compatible EAROM cell," <u>SGS-ATES Componenti Electronici SpA</u> , 7pp. (1982)					
LWH	C11	Caironi et al., "A TV Frequency Synthesis System With A Single Chip Microprocessor Interface Including Non Volatile Memory," <u>IEEE Transactions on Consumer Electronics</u> , Vol. CE-28, No. 3, pp. 363-71 (Aug. 1982)					
LWH	C12	Torelli et al., "Integrating Non-Volatile Station Memory and Remote Control Receiver In A Single Chip," <u>IEEE Digest of Technical Papers</u> , Cat. No. 83CH1872-1, 2pp. (June, 1983)					

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LW		A12	4	3	9	3	4	7	5	7/1983	Kitagawa et al.	365	185.21
LW		A13	4	4	1	5	9	9	2	11/1983	Adlhoch	365	94
LW		A14	4	4	9	5	6	0	2	1/1985	Sheppard	365	104
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		DOCUMENT NUMBER						DATE	COUNTRY	CLASS	SUB CLASS	TRANS.:? (YES/NO)	
OTHER DOCUMENTS (Including Author, Title, Date, Pertinent pages, Etc.)													
LW		C13	Torelli et al., "Non-Volatile Station Memory Single Chip Including Remote Control Receiver and Memory Display Driver," <u>IEEE Transactions on Consumer Electronics</u> , Vol. CE-29, No. 3, pp. 103-13 (Aug. 1983)										
LW		C14	Excerpts from a 1983 Data Book published by SGS-ATES Group, 45 pp. (Nov. 1983)										
LW		C15	Berenga et al., "E <sup>2</sup> -PROM TV Synthesizer," <u>IEEE Digest of Technical Papers</u> , Cat. No. 78CH1298-9SSC, 4 pp. (Feb. 1978)										
LW		C16	Klingman, "Microprocessor Systems Design," <u>Prentice-Hall, Inc.</u> , pp. 30-31 (1977)										
LW		C17	Masuoka et al., "A 256-kbit Flash E <sup>2</sup> PROM Using Triple-Polysilicon Technology," <u>IEEE Journal of Solid-State Circuits</u> , Vol. SC-22, No. 4, (August 1987)										
LW		C18	Bleiker et al., "A Four-State EEPROM Using Floating-Gate Memory Cells," <u>IEEE Journal of Solid-State Circuits</u> , Vol. SC-22, No. 3 (June, 1987)										
LW		C19	Krick, P.J., "Three-State MNOS Fet Memory Array," <u>IBM Technical Disclosure Bulletin</u> , Vol. 18, No. 12, pps. 4192-4193 (May, 1976)										
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<i>RLH</i>	A15	4	8	0	7	1	8	8	2/1989	Casagrande	365	185.25	
<i>RLH</i>	A16	4	9	5	6	8	1	6	9/1990	Atsumi et al.	365	185.22	
<i>RLH</i>	A17	4	9	9	9	8	1	3	5/1991	Ohtsuka et al.	365	185.18	
<b>FOREIGN PATENT DOCUMENTS</b>													
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<b>OTHER DOCUMENTS (Including Author, Title, Date, Pertinent pages, Etc.)</b>													
<i>RLH</i>	C20	Alberts, et al., "Multi-Bit Storage Fet EAROM Cell," <u>IBM Technical Disclosure Bulletin</u> , Vol. 24, No. 7A, pps. 3311-3314 (December 1981)											
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RW	A18 4 8 0 9 2 3 1	2/28/89	Shannon et al.	365	201	
RW	A19 4 7 7 9 2 7 2	10/18/88	Kohda et al.	365	185.2	
RW	A20 4 7 5 2 9 2 9	6/21/88	Kantz et al.	371	21.2	
RW	A21 4 8 7 0 6 1 8	9/26/89	Iwashita	365	185.8	
RW	A22 4 6 1 2 6 2 9	9/16/86	Harari	365	185.08	
RW	A23 4 7 9 9 1 9 5	1/17/89	Iwahashi et al.	365	185.21	
	<del>A24 4 7 3 3 3 9 4</del>	<del>3/22/88</del>	<del>Giebel</del>			
RW	A25 4 2 5 3 0 5 9	2/24/81	Bell et al.	371	21.4	
RW	A26 4 4 6 0 9 8 2	7/17/84	Gee et al.	365	185.19	
	<del>A27 5 1 6 3 0 2 1</del>	<del>11/10/92</del>	<del>Mehrotra et al.</del>			
	<del>A28 5 1 7 2 3 3 0</del>	<del>12/15/92</del>	<del>Mehrotra et al.</del>			

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